|  |  |
| --- | --- |
|  | Self-Biased Sub-1V Bandgap Reference Circuit |
|  |  |
|  | Bilal Ramadan  Supervisor: Dr. Hesham Omran |

Table of Contents

[Part 1: Design Required Specs 3](#_Toc177375633)

[Part 2: BGR Core Circuit 3](#_Toc177375634)

[1. OP simulation 4](#_Toc177375635)

[2. DC temperature sweep simulation 5](#_Toc177375636)

[Part 3: Error Amplifier 6](#_Toc177375637)

[1. OP simulation 7](#_Toc177375638)

[2. DC temperature sweep simulation 8](#_Toc177375639)

[3. Stability analysis 8](#_Toc177375640)

[Part 4: Startup Circuit 9](#_Toc177375641)

[1. OP simulation 10](#_Toc177375642)

[2. Transient analysis supply ramp 11](#_Toc177375643)

[Part 5: Achieved Specs 11](#_Toc177375644)

Tables

[Table 1: Required specs 3](#_Toc177375482)

[Table 2: Achieved specs 11](#_Toc177375483)

Table of Figures

[Figure 1: schematic 3](#_Toc177375492)

[Figure 2: Error amplifier behavioral model 4](#_Toc177375493)

[Figure 3: schematic with DC OP and node voltages annotated 4](#_Toc177375494)

[Figure 4: Vref vs temperature with 0.8 mV change 5](#_Toc177375495)

[Figure 5: Vref across corners with 6 mV change 5](#_Toc177375496)

[Figure 6: schematic 6](#_Toc177375497)

[Figure 7: Error amplifier schematic 6](#_Toc177375498)

[Figure 8: schematic with DC OP and node voltages annotated 7](#_Toc177375499)

[Figure 9: Error amplifier schematic with DC OP and node voltages annotated 7](#_Toc177375500)

[Figure 10: Vref across corners 8](#_Toc177375501)

[Figure 11: Gain crossover frequency 8](#_Toc177375502)

[Figure 12: schematic 9](#_Toc177375503)

[Figure 13: Error amplifier schematic 9](#_Toc177375504)

[Figure 14: schematic with DC OP and node voltages annotated 10](#_Toc177375505)

[Figure 15: Error amplifier schematic with DC OP and node voltages annotated 10](#_Toc177375506)

[Figure 16: Transient Vref across corners at room temperature 11](#_Toc177375507)

# Design Required Specs

|  |  |
| --- | --- |
| Technology |  |
| Supply Voltage |  |
| Change versus Temperature |  |
| Change across Corners |  |
| Current consumption |  |
| Phase margin |  |

Table : Required specs

The Design will be on three phases as follows:

# BGR Core Circuit

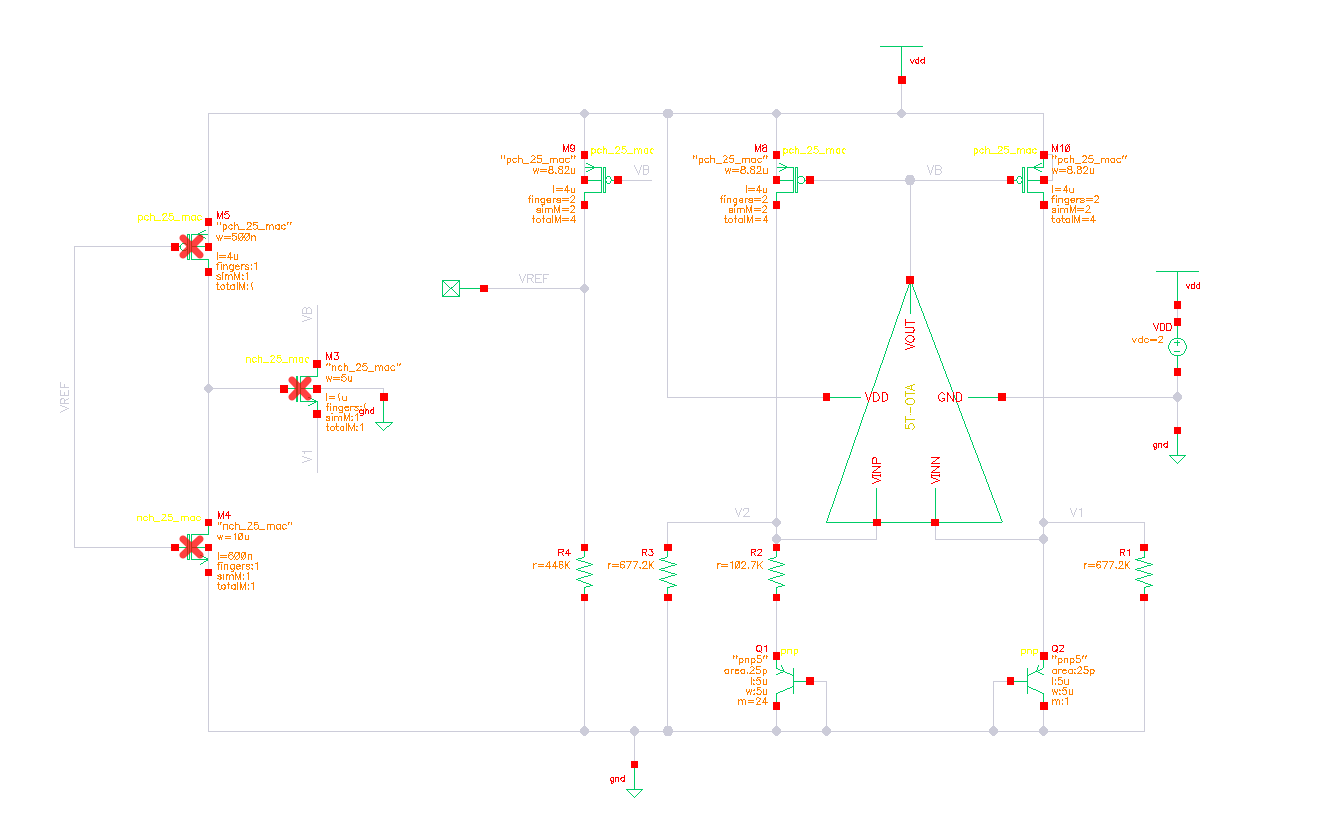


Figure : schematic

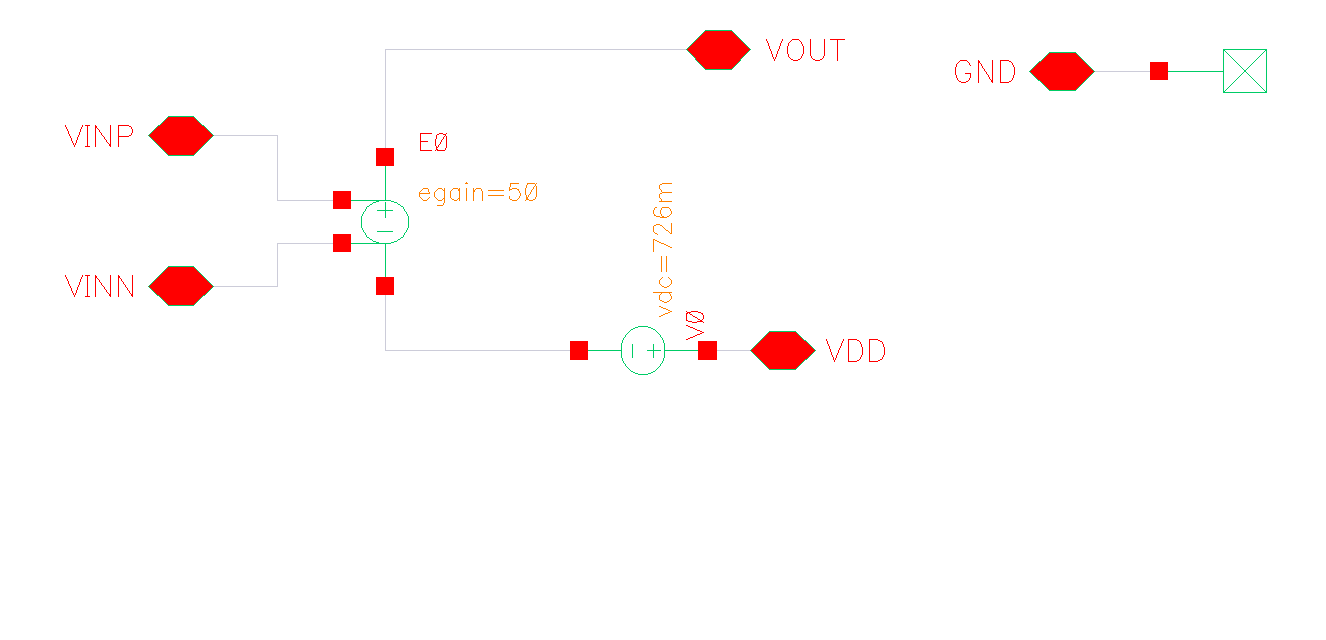


Figure : Error amplifier behavioral model

## OP simulation

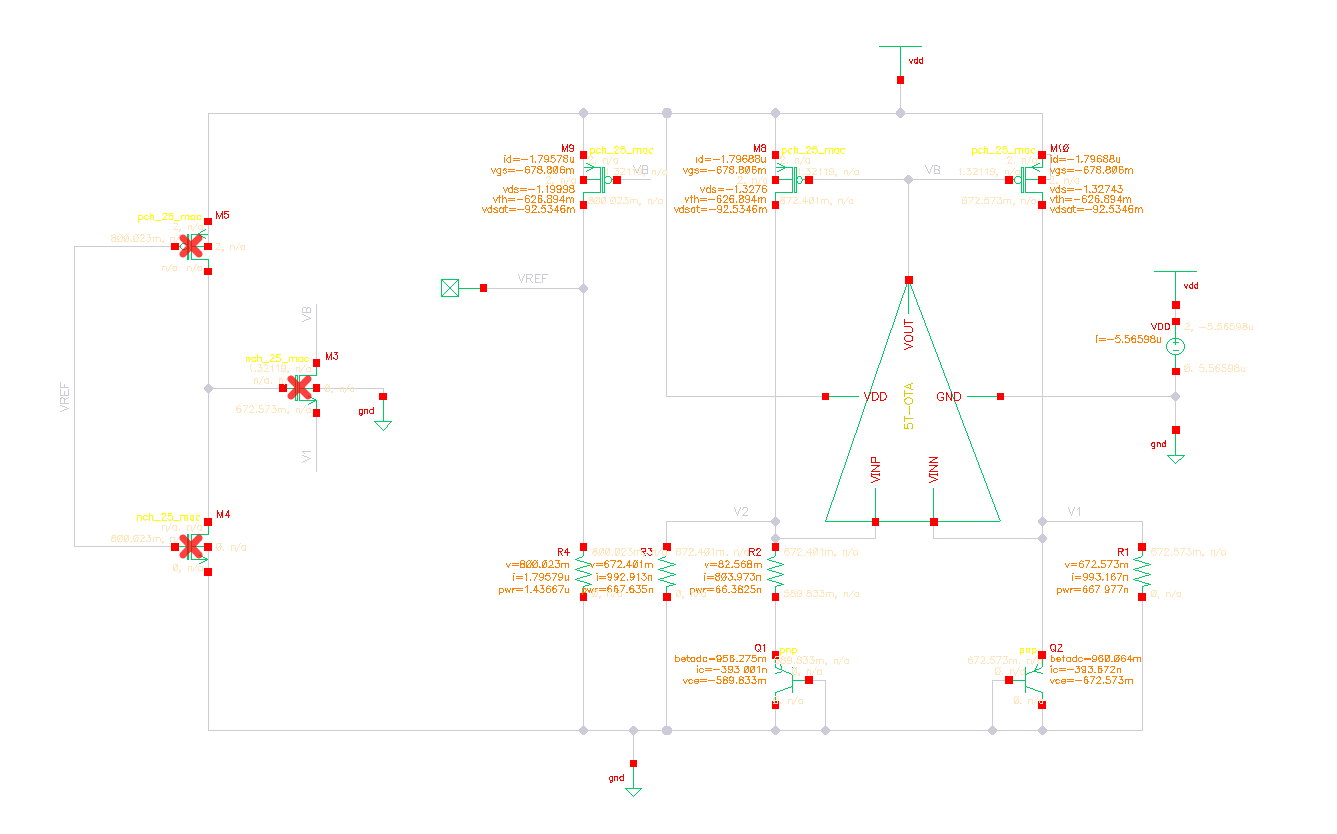


Figure : schematic with DC OP and node voltages annotated

## DC temperature sweep simulation

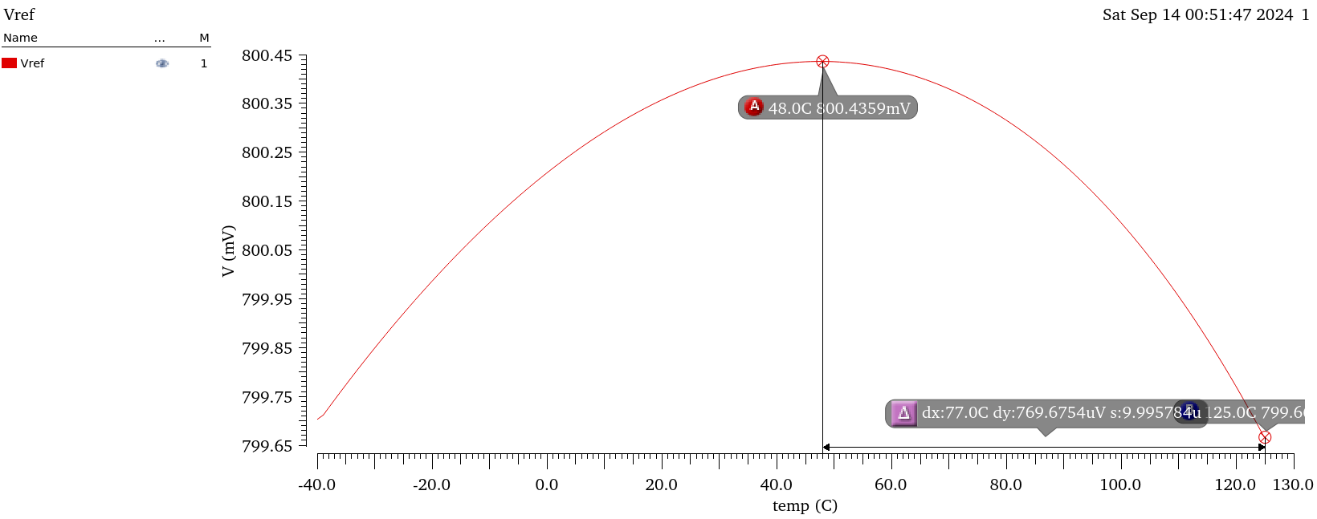


Figure : Vref vs temperature with 0.8 mV change

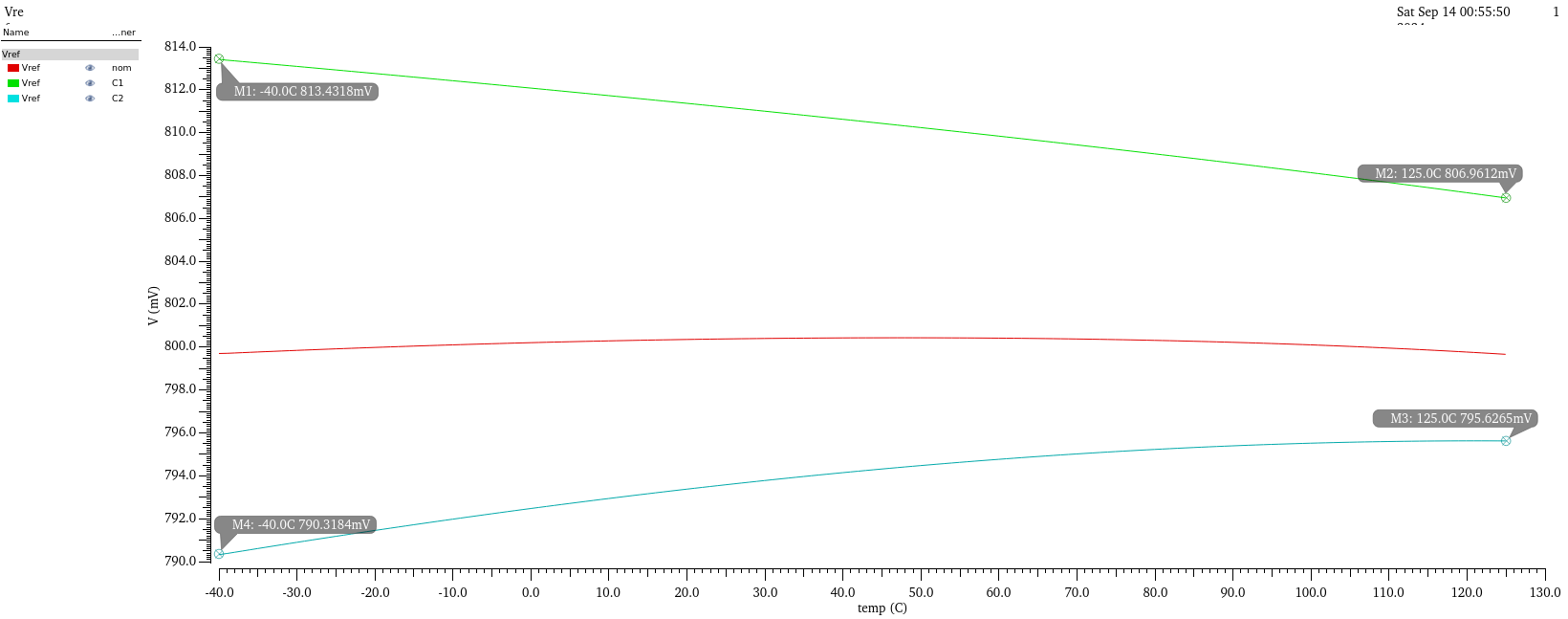


Figure : Vref across corners with 10 mV change

# Error Amplifier

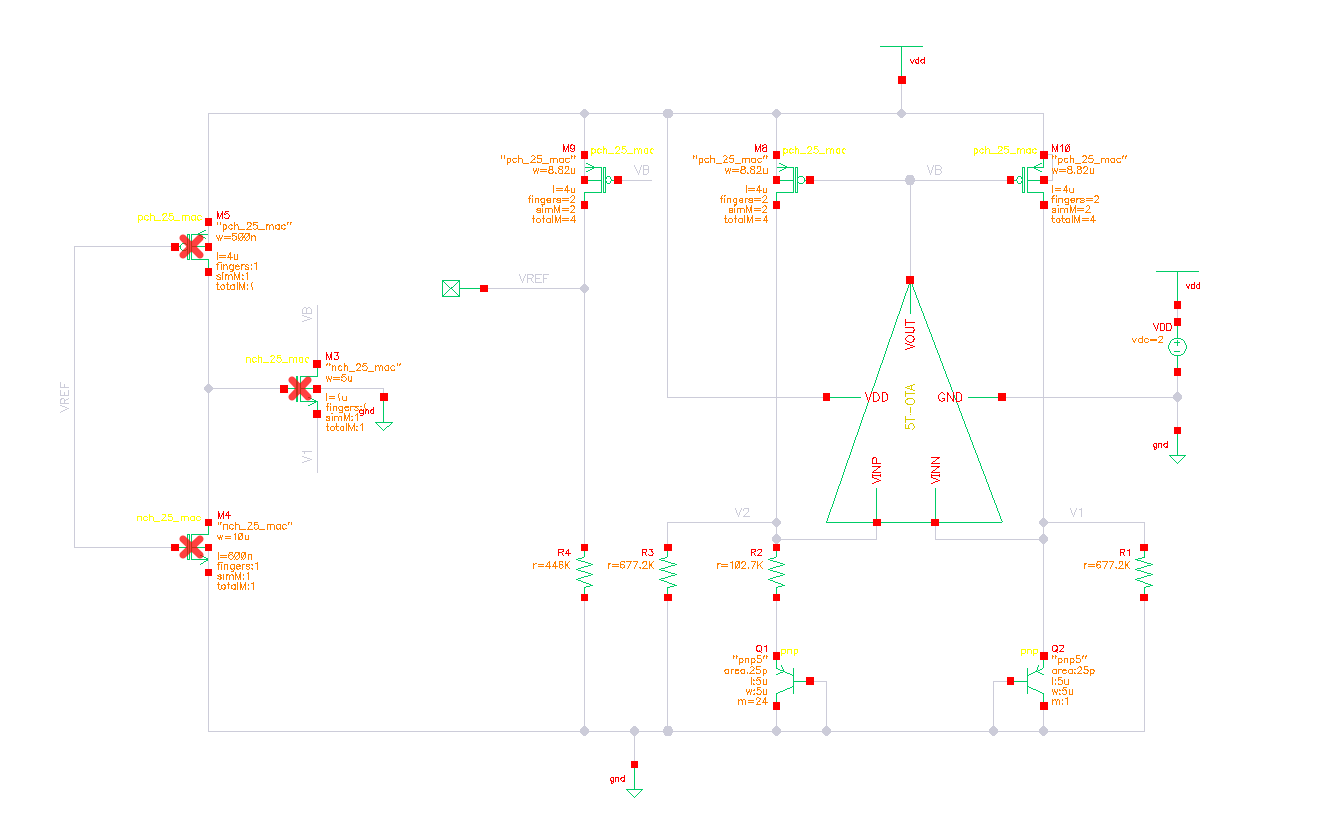


Figure : schematic

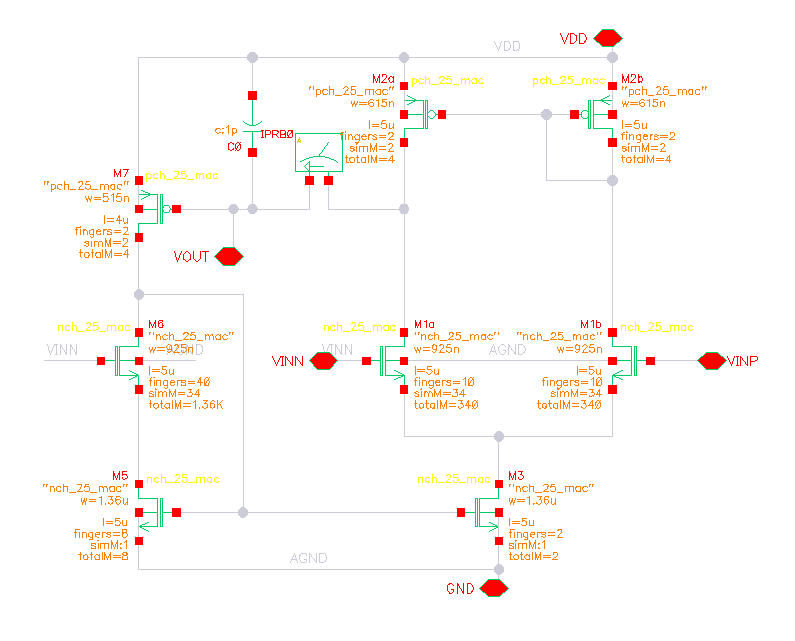


Figure : Error amplifier schematic

## OP simulation

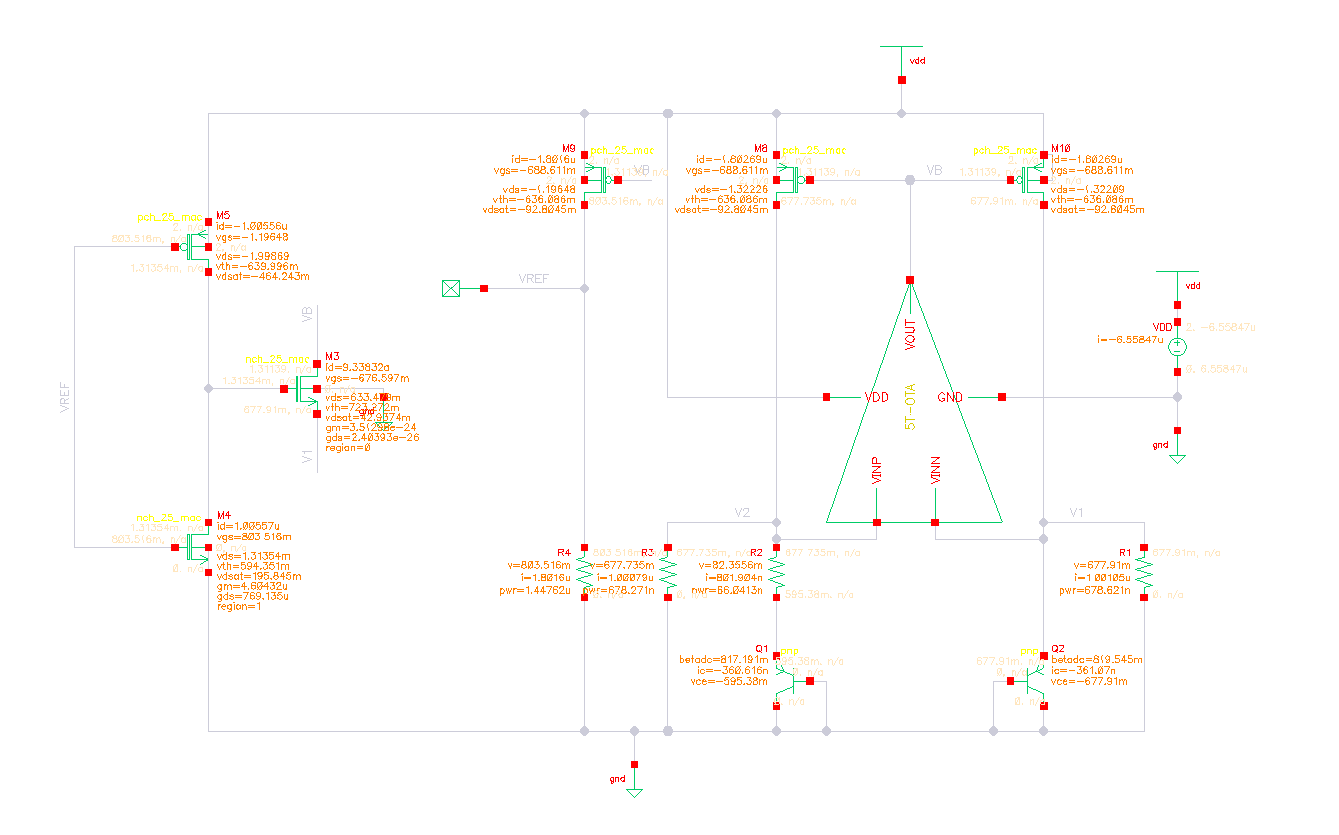


Figure : schematic with DC OP and node voltages annotated

Total power consumption

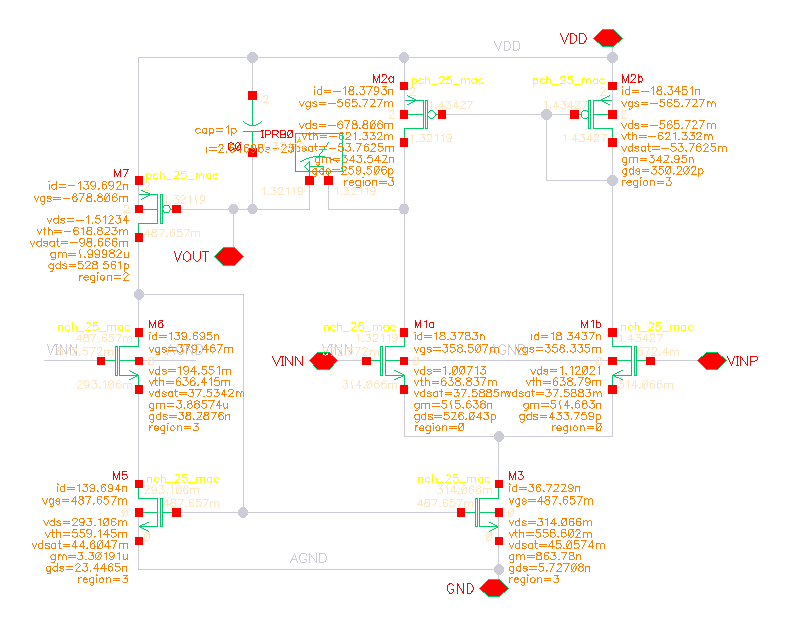


Figure : Error amplifier schematic with DC OP and node voltages annotated

## DC temperature sweep simulation

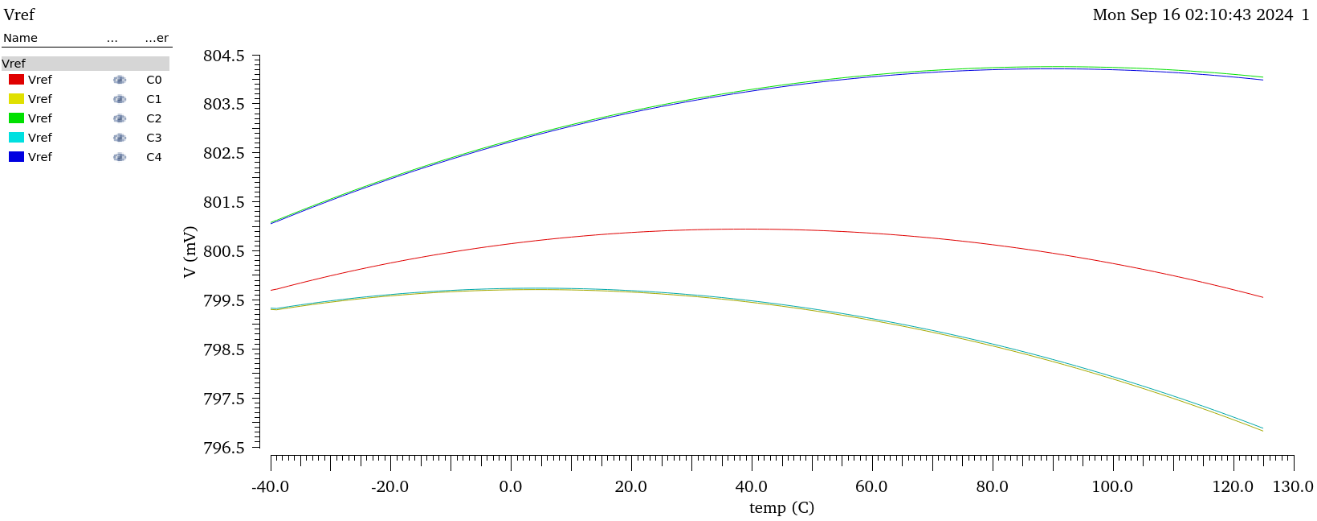


Figure : Vref across corners

## Stability analysis

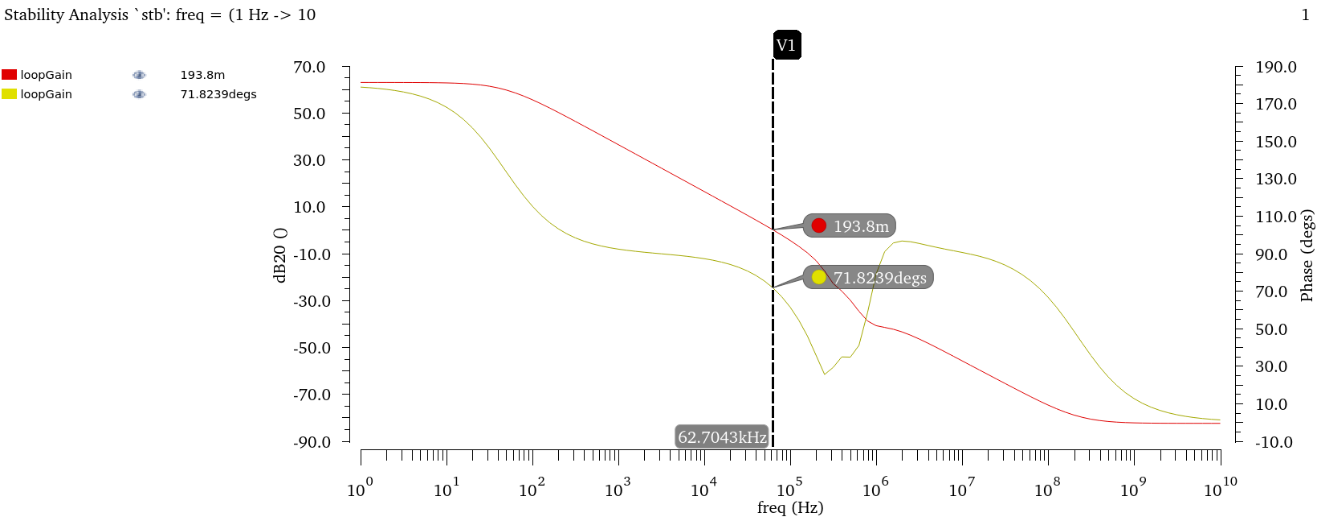


Figure : Gain crossover frequency

# Startup Circuit

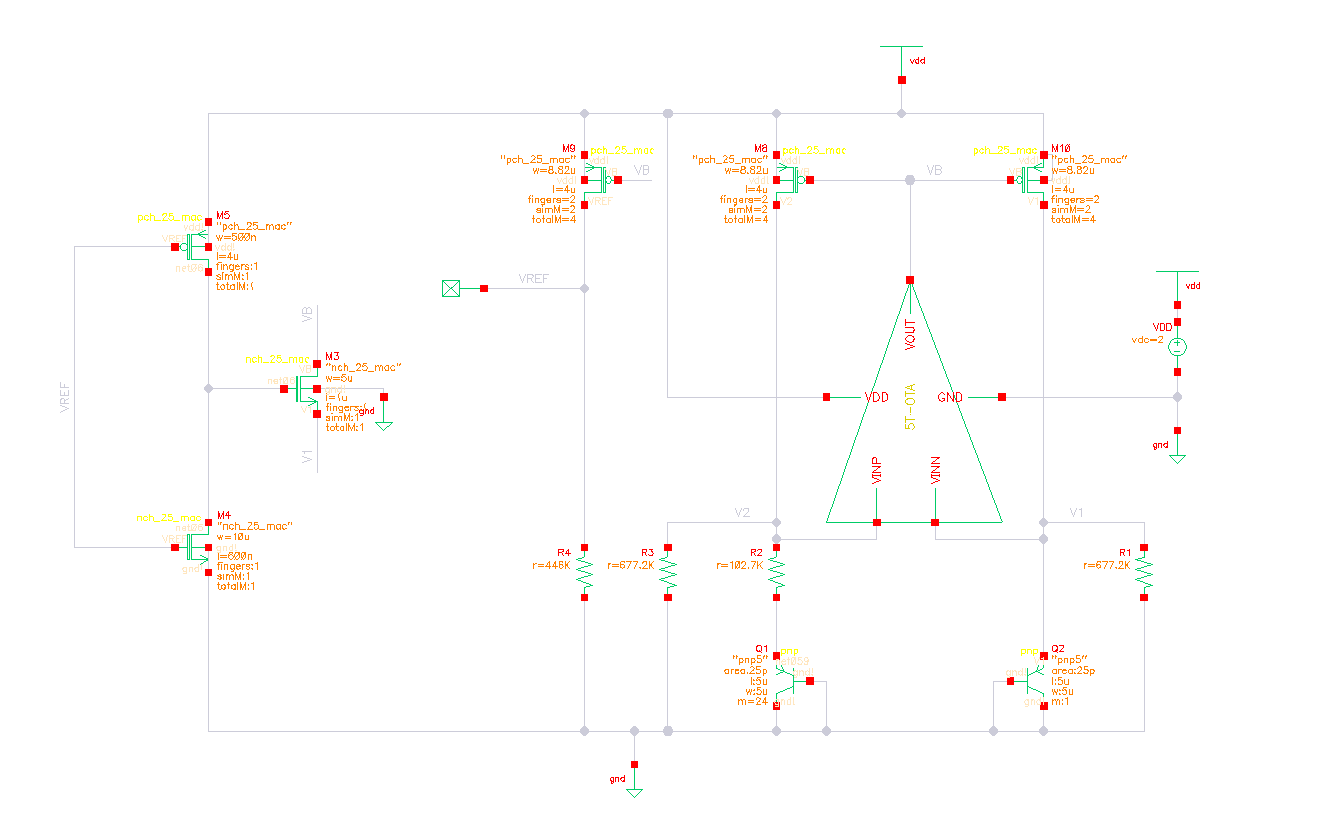


Figure : schematic

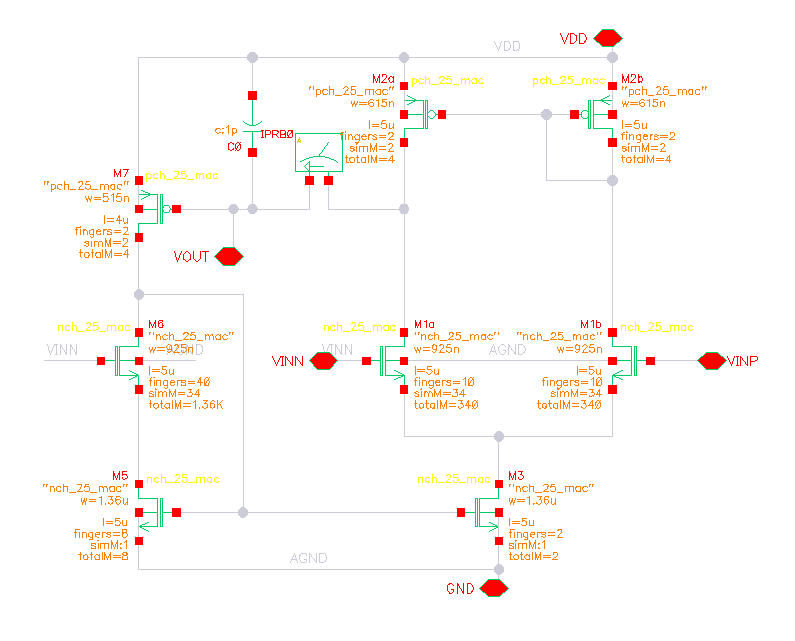


Figure : Error amplifier schematic

## OP simulation

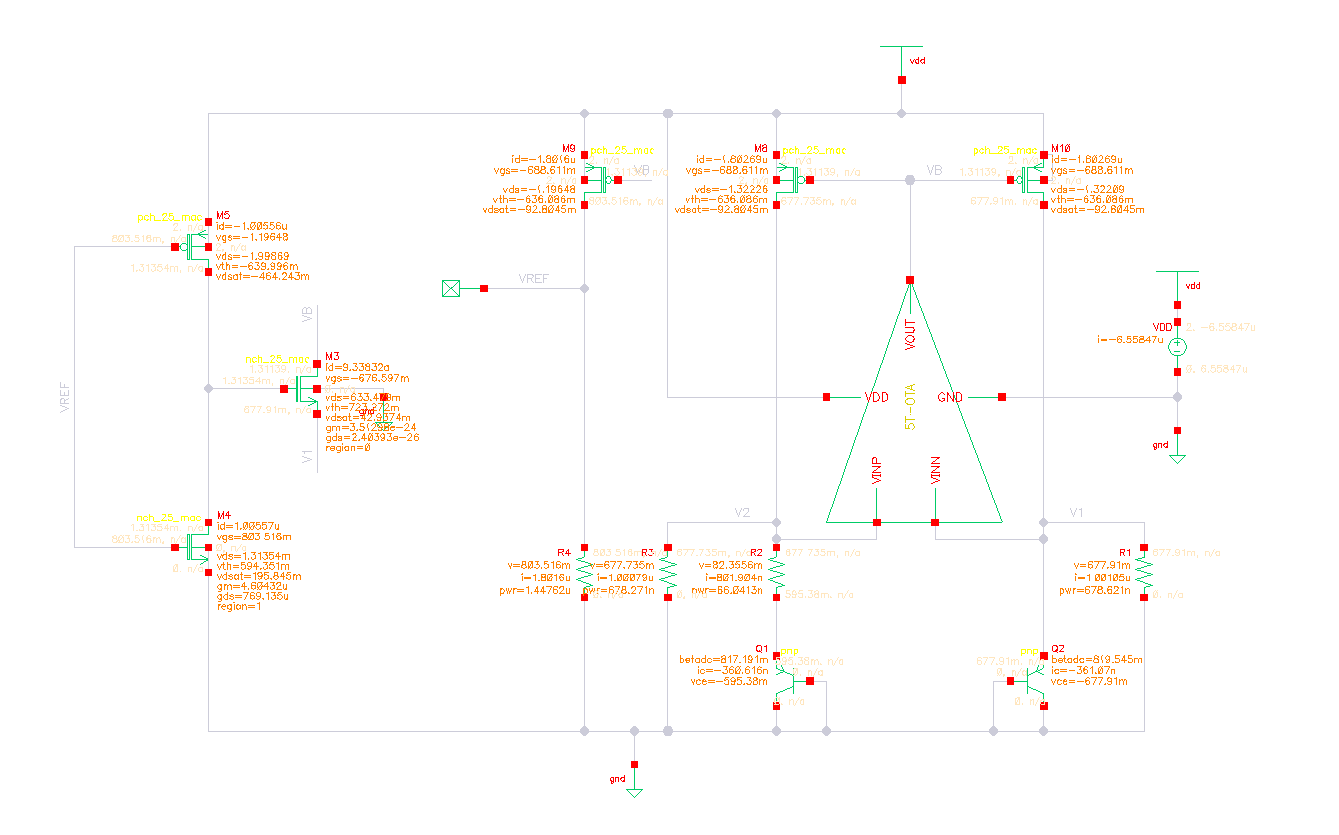


Figure : schematic with DC OP and node voltages annotated

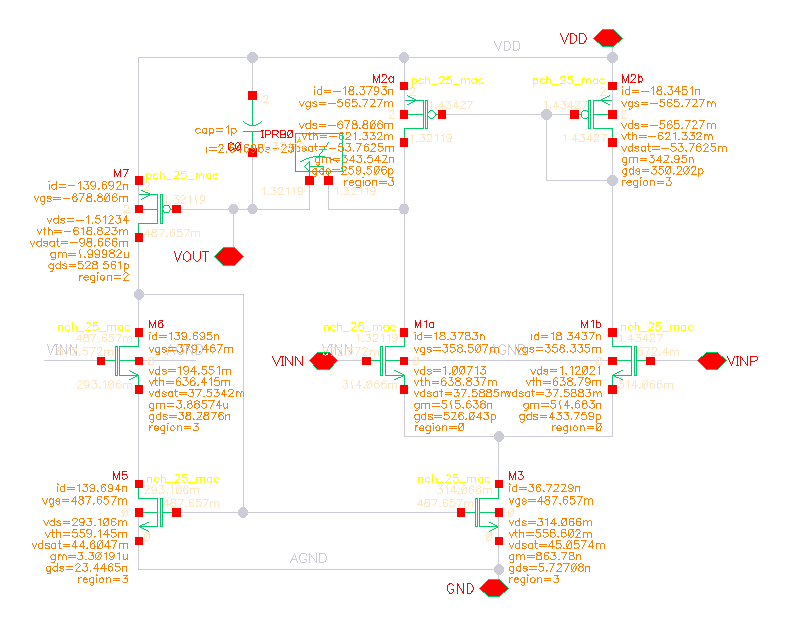


Figure : Error amplifier schematic with DC OP and node voltages annotated

## Transient analysis supply ramp

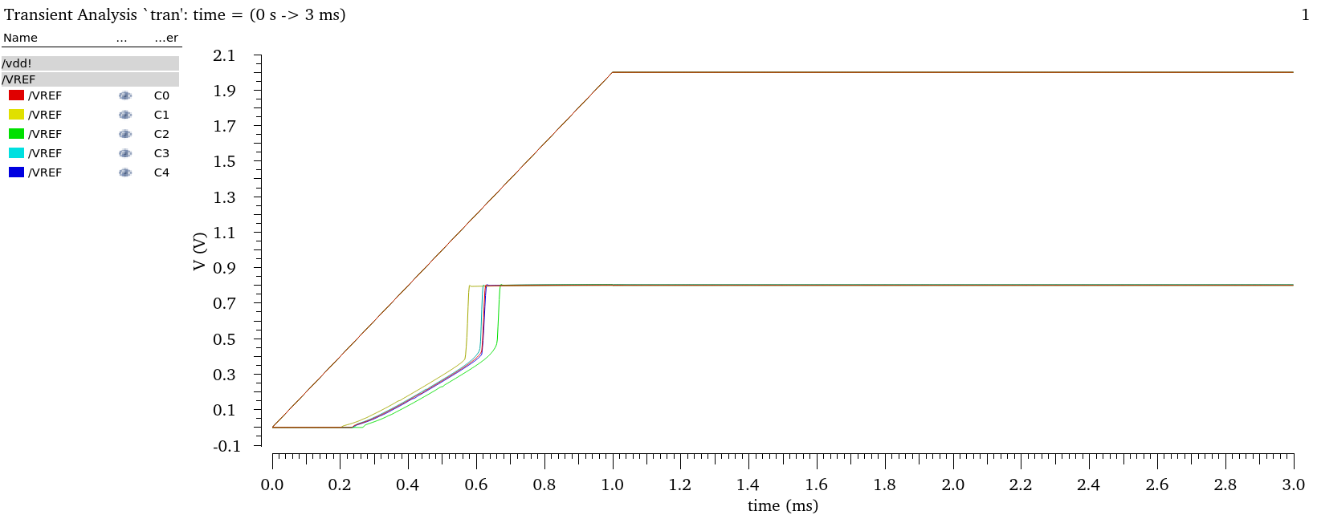


Figure : Transient Vref across corners at room temperature

# Achieved Specs

|  |  |  |
| --- | --- | --- |
| Spec | Required | Achieved |
| Supply Voltage |  |  |
| Change versus Temperature |  |  |
| Change across Corners |  |  |
| Current consumption |  |  |
| Phase margin |  |  |

Table : Achieved specs